AMENDMENTS TO THE CLAIMS

Claims 1-8.(cancelled)

9.(currently amended): An ATM switch system provided at each node in an ATM network, which switches over a working channel to a protection channel, within a protection domain of a duplicated channel segment constituting the working and protection channels, the ATM switch system comprising:

an ATM switch circuit performing a cell switching function;

external line interface portions each inserting cells, located at an external line side;

internal line interface portions each extracting cells, located at an internal line side;

a multiplexer multiplexing cells input from the internal line interface portions and interfacing with the ATM switch circuit;

a demultiplexer interfacing with the ATM switch circuit and demultiplexing multiplexed ATM cells; and

a controller,

wherein the demultiplexer of an ATM switch system of a source node located at a starting point of the protection domain identifies a connection for APS processing, and duplicates cells on a working channel to a protection channel,

an ATM switch system at [[a]] an intermediate node located downstream from the starting point of the protection domain ~~detecting~~ detects a failure on the working channel and transmits an AIS cell in a down stream direction toward an ATM switch system of a destination

node located at a terminal point of the protection domain,

the ATM switch system of the destination node located at the terminal point of the protection domain detects the AIS cell, and transfers it to the controller,

the controller orders the ATM switch system to switch over from an internal line interface portion at which the working channel is terminated, to another internal line interface portion at which the protection channel is terminated, and

the multiplexer allows only ATM cells identified as the connection for APS processing ~~to be transmitted~~, and

wherein the internal line interface in the ATM switch at the intermediate node includes a VPI/VCI converting table, a header modification portion and an alarm cell insertion circuit,

refers to the VPI/VCI converting table using as a reference key an internal channel and a channel identifier for an input ATM cell to obtain an external channel to be output in the external line interface portions and a virtual channel identifier,

sets the obtained virtual channel identifier on the ATM cell at the header modification portion, and

when detecting a failure between the upward starting point and the intermediate node, inserts an alarm cell at the alarm cell insertion circuit according to a control command from the controller.

10.(currently amendmed): The ATM switch system according to claim 9, wherein the demultiplexer in the ATM switch system of [[a]] the source node located at an upward starting

point of the protection domain includes a cell copy table storing information of an output line to be used for a protection channel [[and]] of a channel in the output line,

identifies an identifier in a header of an input cell, indicating whether or not the input cell is of a connection for APS processing,

when the identifier indicates the input cell is of the connection for APS processing, refers to the cell copy table, using as a reference key an identifier identifying a channel in a output line specified by a Tag to obtain information on an output line to be used for a protection channel and a channel in the output line, and

duplicates the input cell, sets in the duplicated cell the obtained information on an output line to be used for a protection channel and a channel in the output line and outputs the duplicated cell.

11.(cancelled)

12.(currently amended): The ATM switch system according to claim 9, wherein the internal line interface in an ATM switch at [[a]] the destination node located at a downstream terminating point of the protection domain includes a VPI/VCI conversion table, a header modification portion, APS bit set table, and ACT bit set table,

refers to the VPI/VCI conversion table by using a channel and a virtual channel identifier provided in an input ATM cell as a reference key to obtain an internal channel and a virtual channel identifier,

converts the obtained internal channel and virtual channel identifier to a

condensed internal channel and virtual channel identifier,

modifies the header portion of the input ATM cell with the obtained and condensed internal channel and virtual channel identifier,

refers to the APS bit set table by using as a reference key the obtained and condensed internal channel and virtual channel identifier, to determine whether the internal channel and virtual channel identifier are an object for APS processing according to a referenced APS bit,

refers to the ACT bit set table by using as a reference key the condensed internal channel and virtual channel identifier, to determine whether or not a cell determined for APS processing is a cell to be transmitted to a user, and

modifies the header of the ATM cell with the APS bit and the ACT bit at the header modification portion to output the ATM cell.

13.(previously presented): The ATM switch system according to claim 12, further comprising an ACT bit set table in which an ACT bit is set in group unit; and

an APS group conversion table and an APS identifier set table, wherein the condensed internal channel and channel identifier are used to refer to the APS group conversion table, and the APS group obtained from the APS group conversion table is used to refer to the ACT bit set table.

14.(previously presented): The ATM switch system according to claim 13, wherein the multiplexer includes cell invalidation circuits each corresponding to a channel route, and only

cells to which the ACT bit is set ON in the protection channel are transmitted through the cell invalidation circuits.

15.(previously presented): The ATM switch system according to claim 9, wherein the multiplexer includes cell invalidation circuits each corresponding to a channel route, and only cells to which the ACT bit is set ON in the protection channel are transmitted through the cell invalidation circuits.

16.(previously presented): The ATM switch system according to claim 10, wherein the multiplexer includes cell invalidation circuits each corresponding to a channel route, and only cells to which the ACT bit is set ON in the protection channel are transmitted through the cell invalidation circuits.

17.(cancelled)

18.(previously presented): The ATM switch system according to claim 12, wherein the multiplexer includes cell invalidation circuits each corresponding to a channel route, and only cells to which the ACT bit is set ON in the protection channel are transmitted through the cell invalidation circuits.